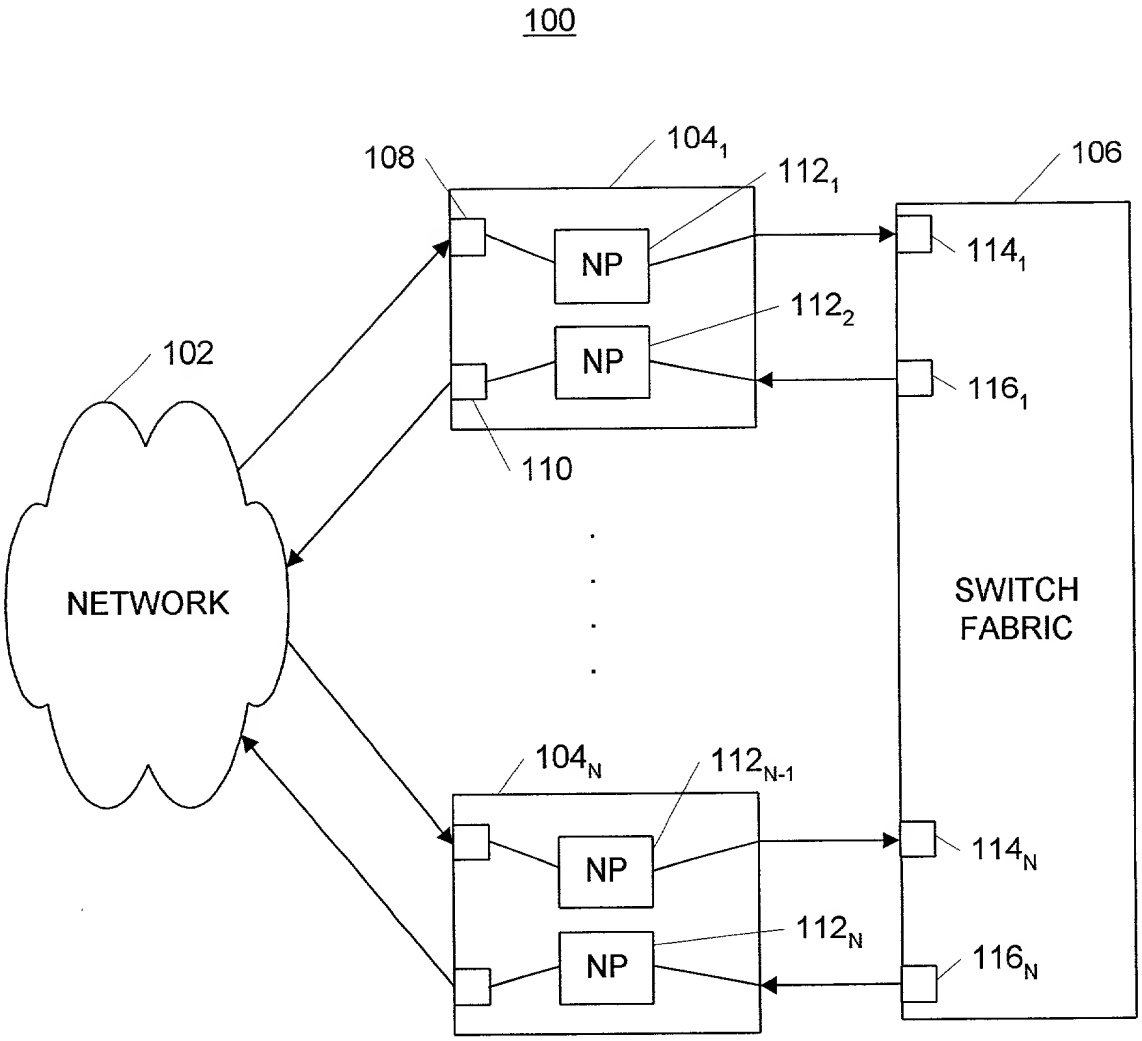

100
108
104_1
112_1
106
NP
114_1
112_2
NP
102
116_1
110
NETWORK
SWITCH
FABRIC
104_N
112_{N-1}
NP
114_N
112_N
NP
116_N

FIG. 1

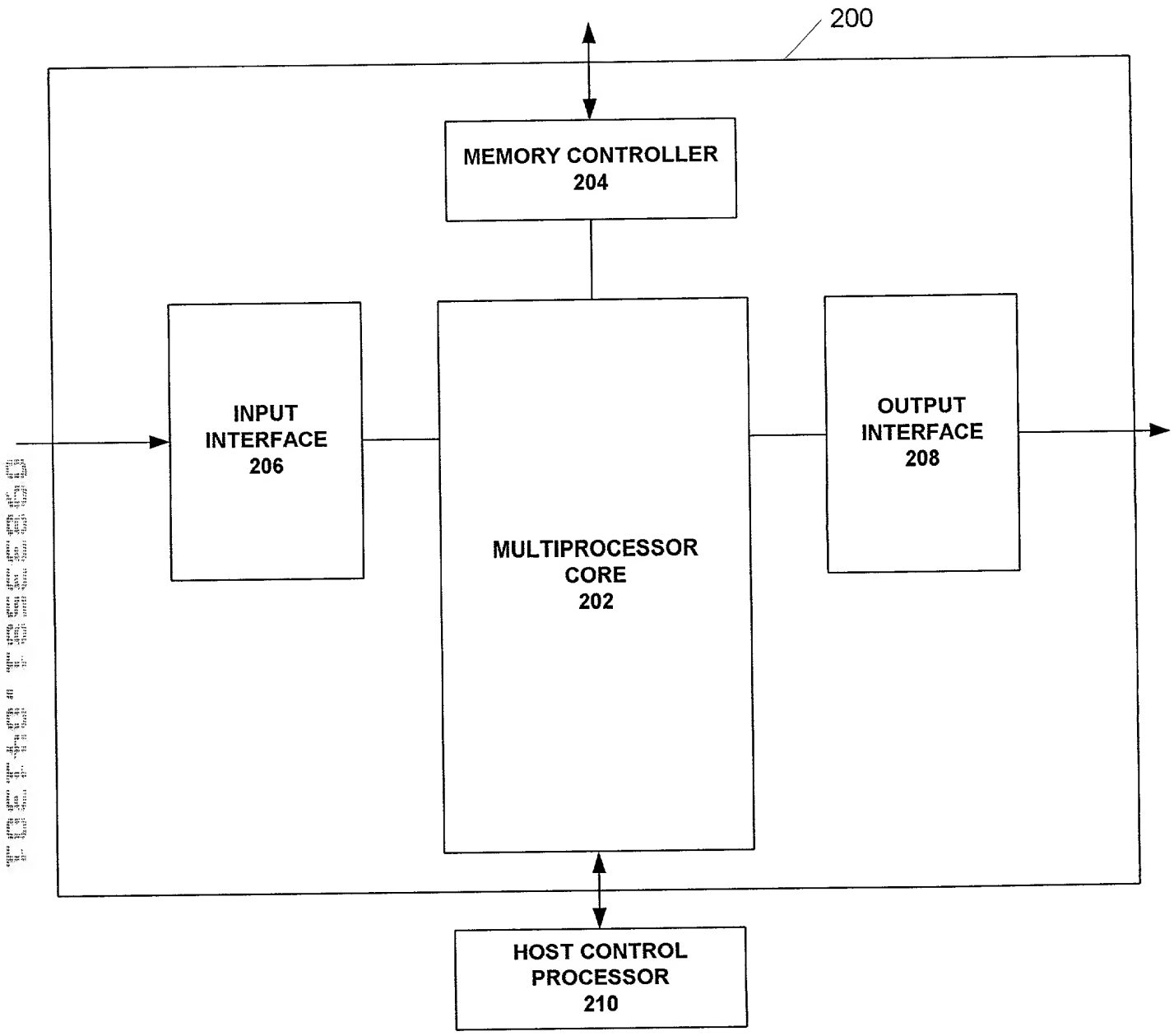

200
MEMORY CONTROLLER
204
INPUT
INTERFACE
206
MULTIPROCESSOR
CORE
202
OUTPUT
INTERFACE
208
HOST CONTROL
PROCESSOR
210

FIG. 2

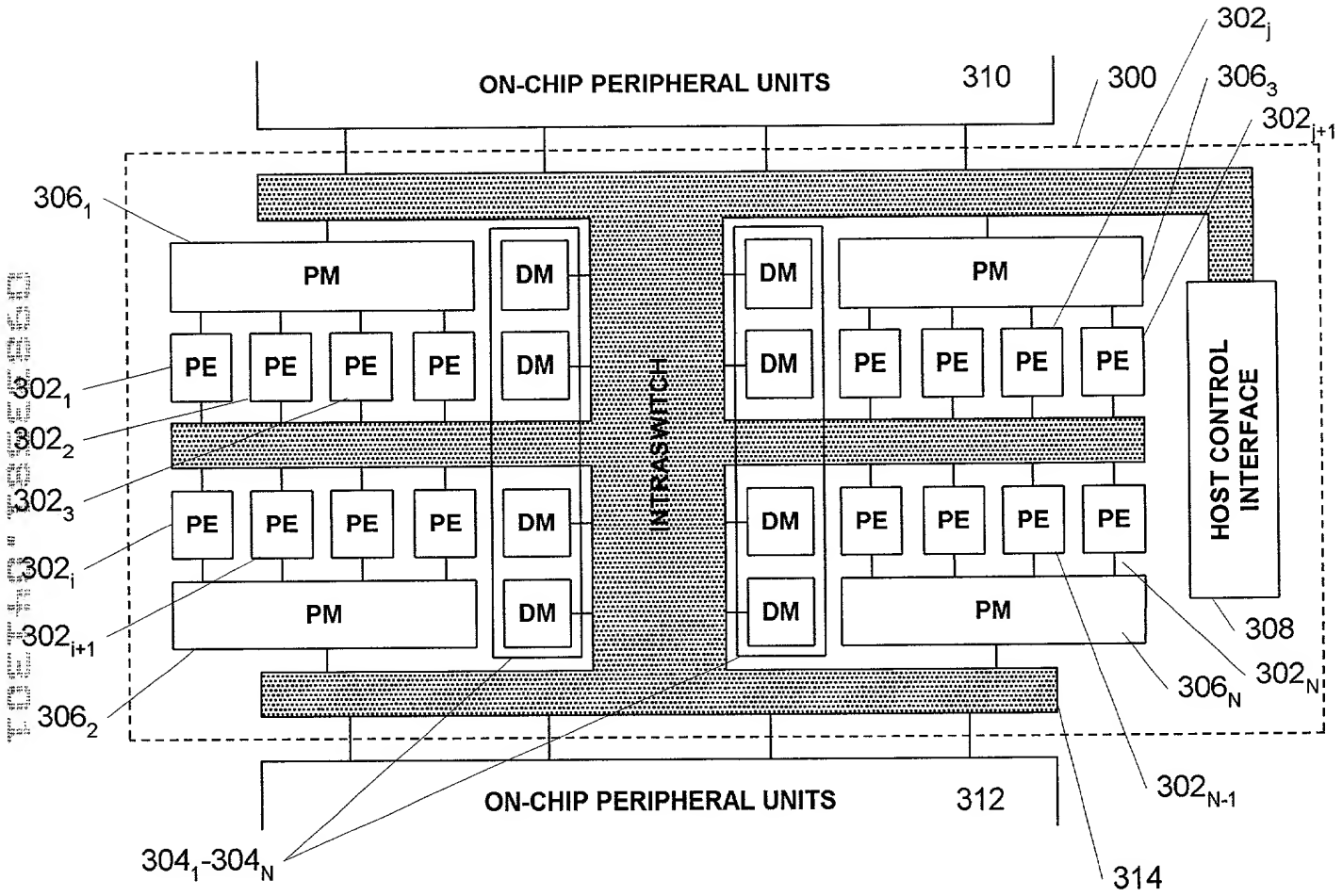

ON-CHIP PERIPHERAL UNITS
310
300
302_j
306_3
302_{j+1}
306_1
PM
DM
PE
302_1
302_2
302_3
302_i
302_{i+1}
306_2
INTRA SWITCH
HOST CONTROL INTERFACE
308
306_N
302_N
302_{N-1}
ON-CHIP PERIPHERAL UNITS
312
304_1-304_N
314
PM: PROGRAM MEMORY
DM: DATA MEMORY
PE: PROCESSING ELEMENT

FIG. 3

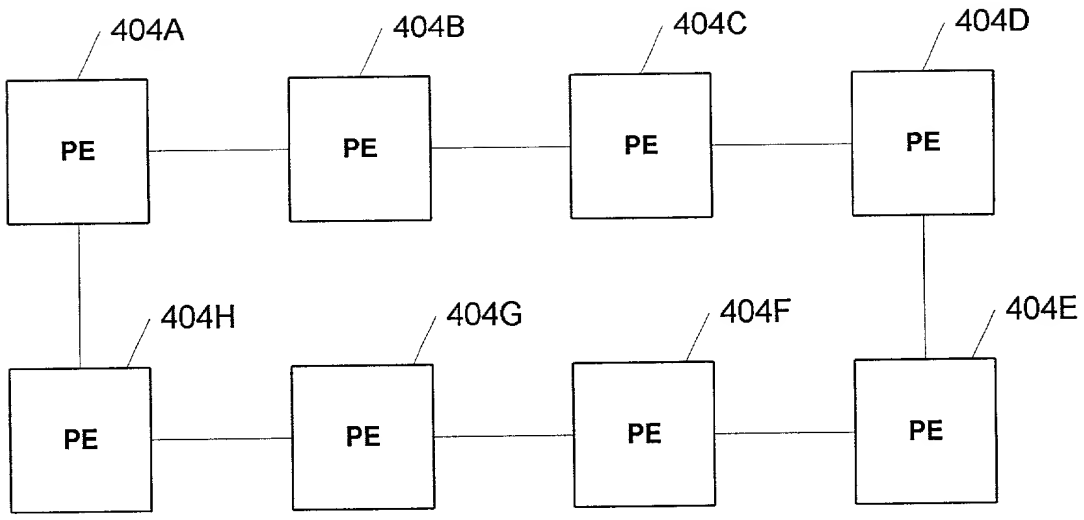

404A
404B
404C
404D
PE
PE
PE
PE
404H
404G
404F
404E
PE
PE
PE
PE

FIG. 4A

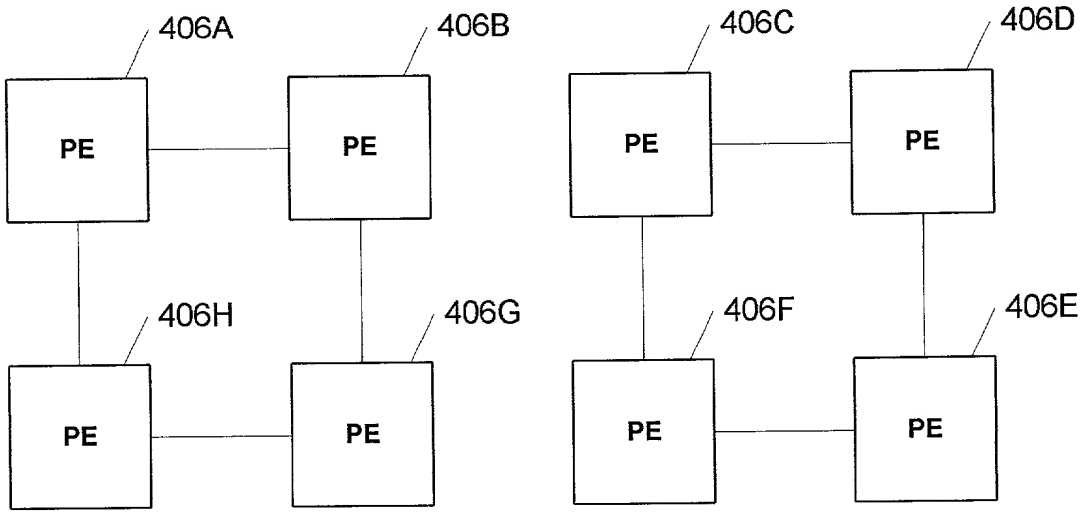

406A
406B
406C
406D
PE
PE
PE
PE
406H
406G
406F
406E
PE
PE
PE
PE

FIG. 4B

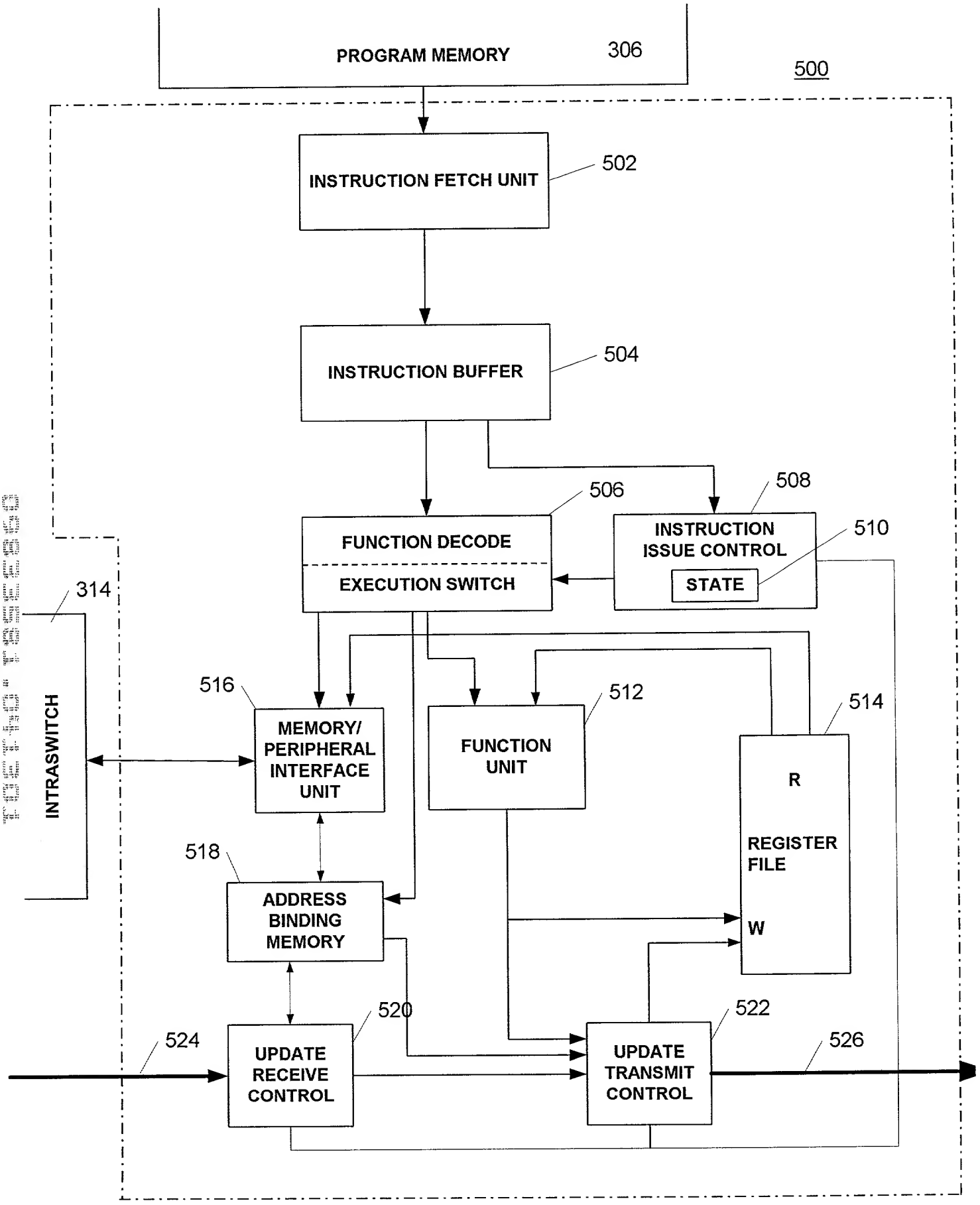

PROGRAM MEMORY
306
500
INSTRUCTION FETCH UNIT
502
INSTRUCTION BUFFER
504
FUNCTION DECODE
EXECUTION SWITCH
506
INSTRUCTION ISSUE CONTROL
STATE
508
510
314
INTRASWITCH
516
MEMORY/ PERIPHERAL INTERFACE UNIT
FUNCTION UNIT
512
514
R
REGISTER FILE
W
518
ADDRESS BINDING MEMORY
520
522
524
UPDATE RECEIVE CONTROL
UPDATE TRANSMIT CONTROL
526

FIG. 5

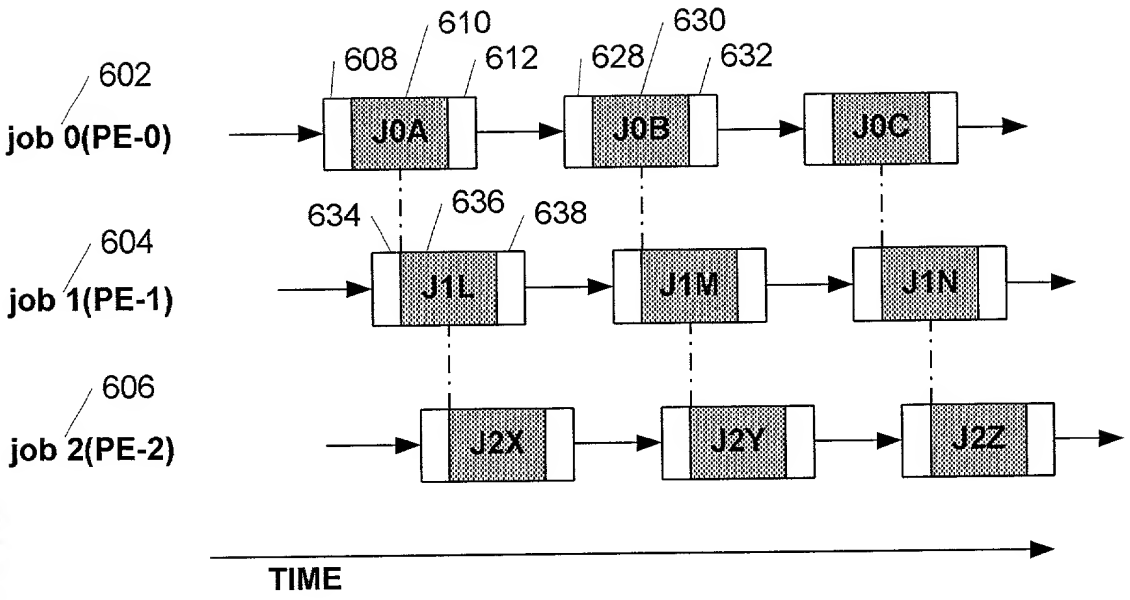

600
602
job 0(PE-0)
608
610
612
J0A
628
630
632
J0B
J0C
634
636
638
604
job 1(PE-1)
J1L
J1M
J1N
606
job 2(PE-2)
J2X
J2Y
J2Z
TIME

FIG. 6

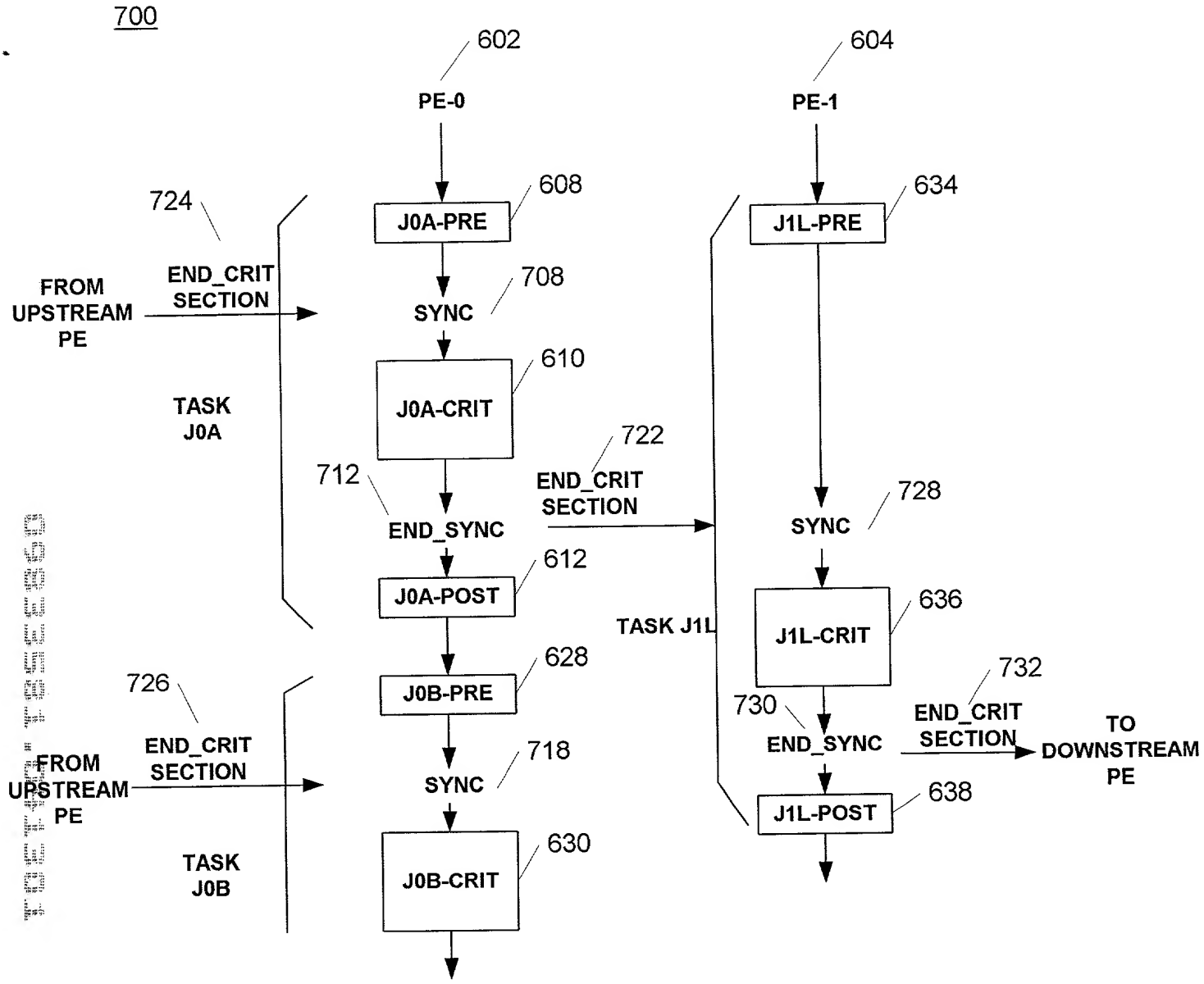

700
602
PE-0
604
PE-1
724
608
J0A-PRE
634
J1L-PRE
FROM UPSTREAM PE
END_CRIT SECTION
708
SYNC
610
J0A-CRIT
TASK J0A
722
712
END_CRIT SECTION
END_SYNC
728
SYNC
612
J0A-POST
636
J1L-CRIT
TASK J1L
628
J0B-PRE
732
730
END_CRIT SECTION
TO DOWNSTREAM PE
726
END_CRIT SECTION
FROM UPSTREAM PE
718
SYNC
END_SYNC
638
J1L-POST
630
J0B-CRIT
TASK J0B

FIG. 7

800

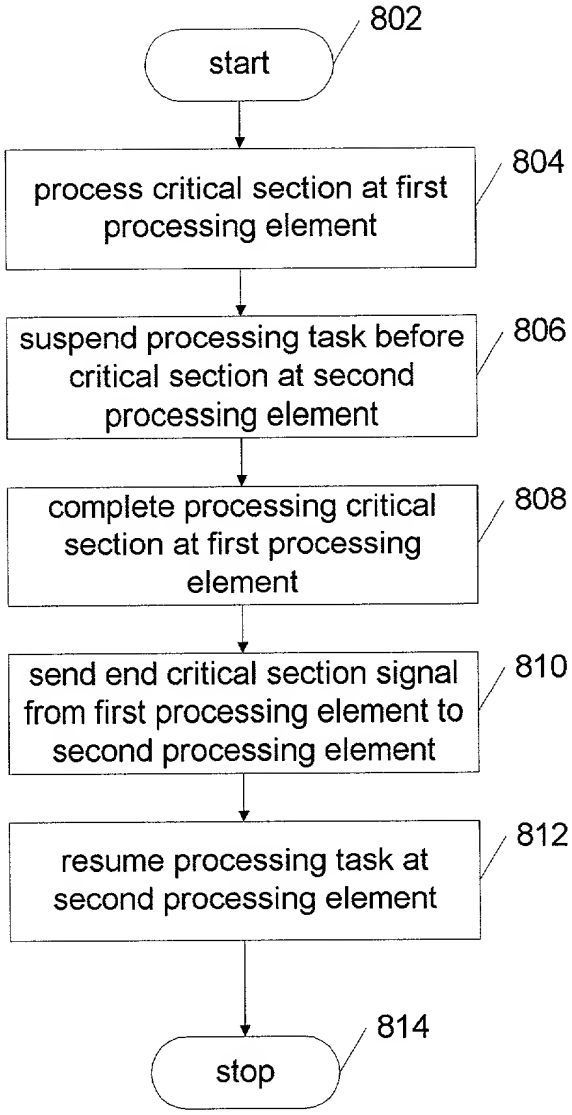

802
start
804
process critical section at first processing element
806
suspend processing task before critical section at second processing element
808
complete processing critical section at first processing element
810
send end critical section signal from first processing element to second processing element
812
resume processing task at second processing element
814
stop

FIG. 8

900

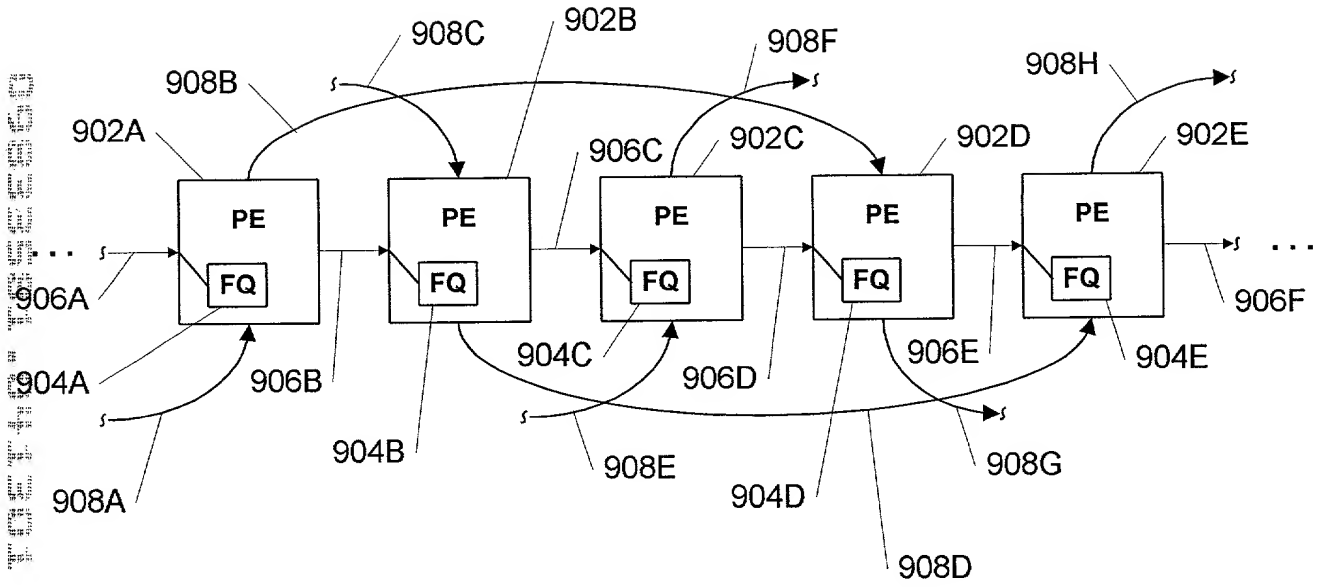
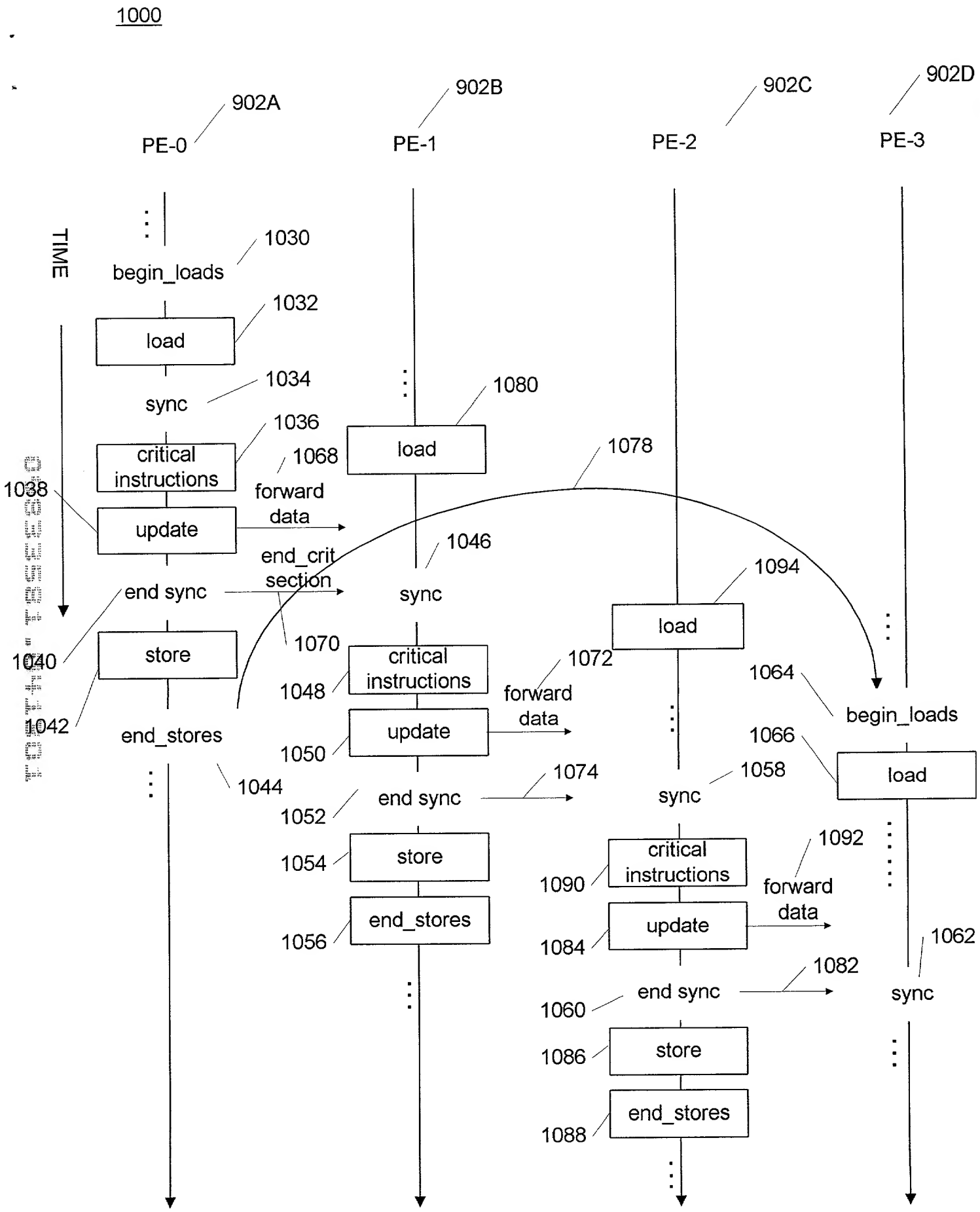

908C
902B
908F
908H
908B
902A
906C
902C
902D
902E
PE
FQ
906A
906F
904A
906B
904C
906D
906E
904E
908A
904B
908E
904D
908G
908D

FIG. 9

FIG. 10


1000
902A
902B
902C
902D
PE-0
PE-1
PE-2
PE-3
TIME
1030
begin_loads
1032
load
1034
sync
1036
critical instructions
1038
update
1040
end sync
1042
store
1044
end_stores
1068
forward data
1070
end_crit section
1078
1080
load
1046
sync
1048
critical instructions
1050
update
1052
end sync
1054
store
1056
end_stores
1072
forward data
1074
1094
load
1058
sync
1090
critical instructions
1084
update
1060
end sync
1086
store
1088
end_stores
1064
begin_loads
1066
load
1092
forward data
1082
1062
sync

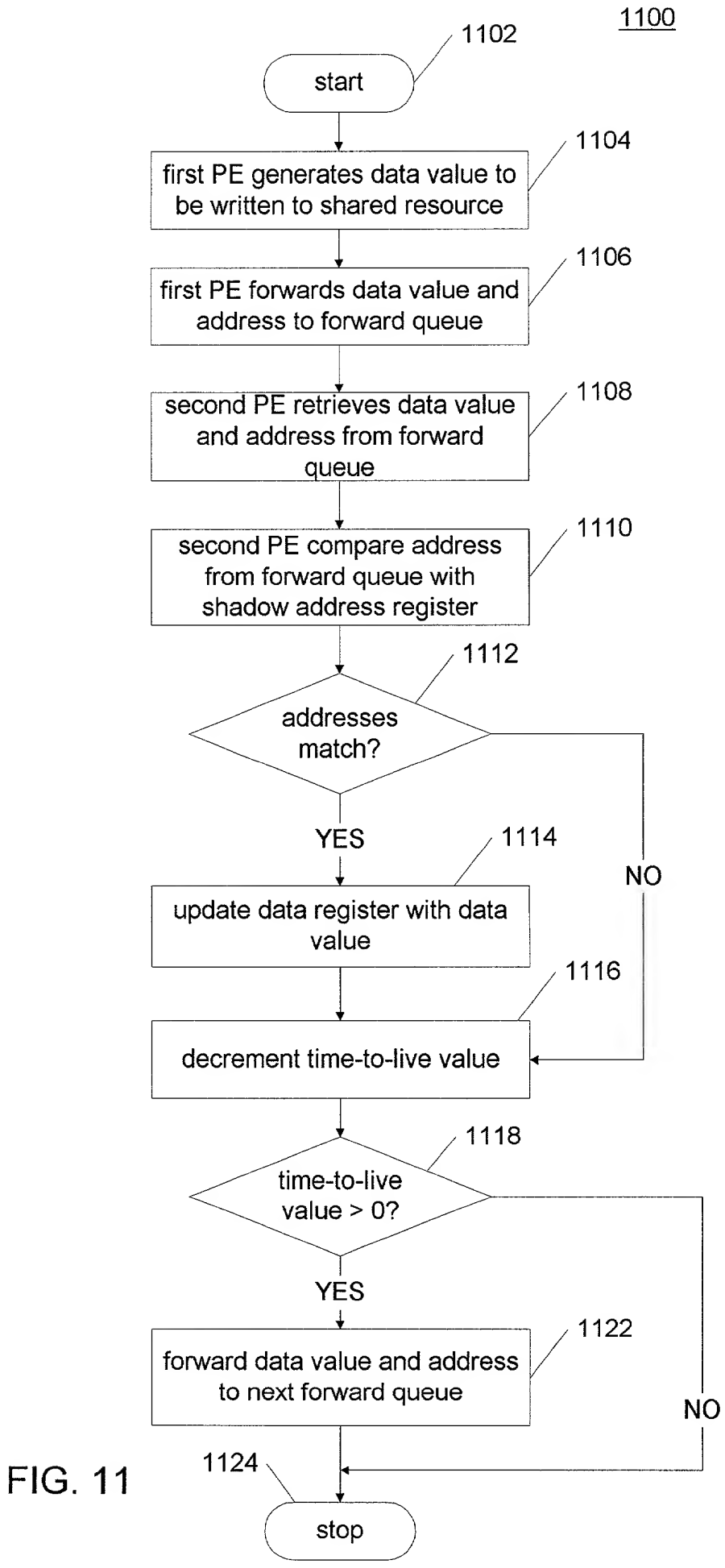
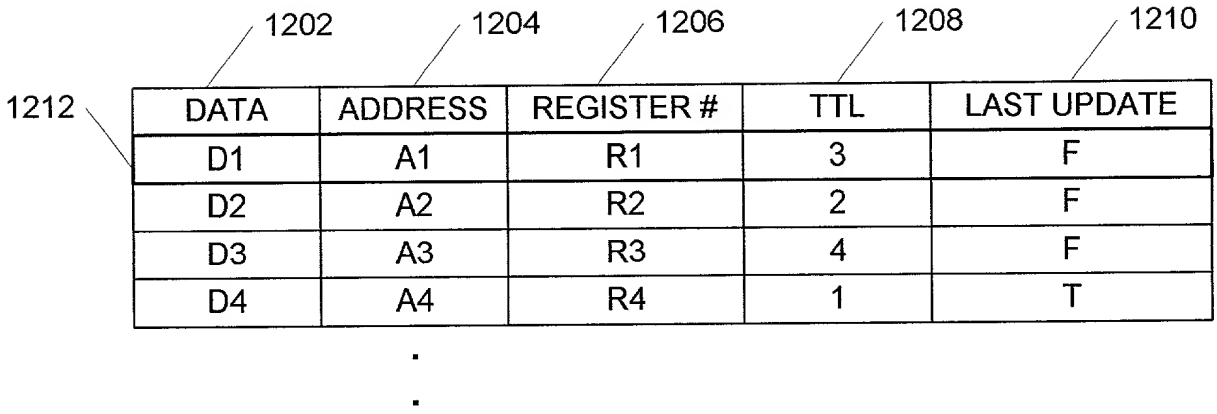

1100
1102
start
1104
first PE generates data value to be written to shared resource
1106
first PE forwards data value and address to forward queue
1108
second PE retrieves data value and address from forward queue
1110
second PE compare address from forward queue with shadow address register
1112
addresses match?
YES
NO
1114
update data register with data value
1116
decrement time-to-live value
1118
time-to-live value > 0?
YES
NO
1122
forward data value and address to next forward queue
1124
stop

FIG. 11

1200



DATA	ADDRESS	REGISTER #	TTL	LAST UPDATE
D1	A1	R1	3	F
D2	A2	R2	2	F
D3	A3	R3	4	F
D4	A4	R4	1	T

FIG. 12

1300

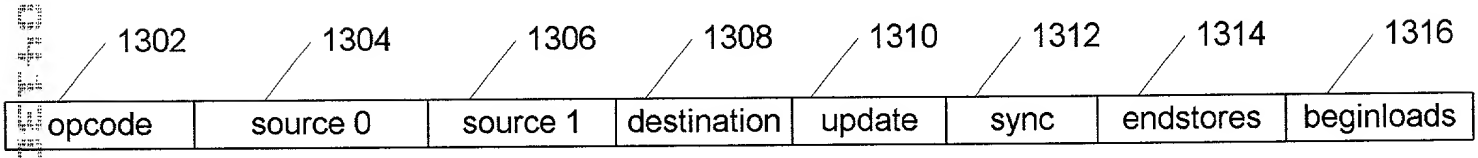


FIG. 13